AMENDMENT TO THE CLAIMS

1-12. (Canceled)

13. (Currently amended) A semiconductor device, comprising on the same semiconductor substrate:

a first DRAM section including a first memory cell having a first capacitive element having a first capacitance; and

a second DRAM section including a second memory cell having a second capacitive element having a second capacitance [[different from]] larger than the first capacitance, ~~the first DRAM section and the second DRAM section being provided on the same semiconductor substrate,~~

wherein the [[first memory cell has a]] first capacitive element [[including]] includes:

a first capacitor lower electrode composed of a first diffusion layer formed in the semiconductor substrate; [[,]]

a first capacitor insulating film formed on the first capacitor lower electrode; [[,]] and

a first capacitor upper electrode formed on the first capacitor insulating film,

the [[second memory cell has a]] second capacitive element [[including]] includes:

a second capacitor lower electrode composed of a conductive film formed on an insulating film provided on the semiconductor substrate; [[,]]

a second capacitor insulating film formed on the second capacitor lower electrode; [[,]] and

a second capacitor upper electrode formed on the second capacitor insulating film, and

an operating voltage of the first DRAM section is [[different from]] higher than an operating voltage of the second DRAM section.

14. (Canceled)

15. (Previously Presented) The semiconductor device of claim 13, wherein the surface area of the second capacitor lower electrode is larger than the surface area of the first capacitor lower electrode.

16. (Canceled)

17. (Previously Presented) The semiconductor device of claim 13, wherein the first capacitive element has a structure of a planar capacitor, and

the second capacitive element has a structure of a stacked capacitor.

18. (Canceled)

19. (Previously Presented) The semiconductor device of claim 13, wherein the first DRAM section and the second DRAM section are formed on the same chip.

20. (Previously Presented) The semiconductor device of claim 13, wherein charge stored in the first capacitive element is smaller than charge stored in the second capacitive element.

21. (Currently amended) The semiconductor device of claim 13, wherein the first memory cell includes a first gate insulating film formed on the semiconductor substrate, [[and]] a first gate electrode formed on the first gate insulating film, and a second diffusion layer formed in regions located on both sides of the first gate electrode in the semiconductor substrate,

the first diffusion layer is connected to the second diffusion layer, and

the first capacitor insulating film is made of the same insulating film as the first gate insulating film.

22. (New) The semiconductor device of claim 13, wherein the second memory cell includes a second gate insulating film formed on the semiconductor substrate, a second gate electrode formed on the second gate insulating film, and a third diffusion layer formed in regions located on both sides of the second gate electrode in the semiconductor substrate, and

the insulating film is provided with a contact plug connecting the third diffusion layer to the second capacitor lower electrode.